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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,149	12/15/2003	Young-Dong Nam	SAM-0476	6342
7590	10/17/2005		EXAMINER	LE, JOHN H
Steven M. Mills MILLS & ONELLO LLP Suite 605 Eleven Beacon Street Boston, MA 02108			ART UNIT	PAPER NUMBER
			2863	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	10/737,149	
Examiner	NAM, YOUNG-DONG	
John H. Le	Art Unit 2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 24 August 2005.
2a) This action is **FINAL**. 2b) This action is non-final.
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-6 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) Claim(s) _____ is/are allowed.
6) Claim(s) 1-6 is/are rejected.
7) Claim(s) _____ is/are objected to.
8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
10) The drawing(s) filed on 15 December 2003 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____

Response to Amendment

1. This office action is in response to applicant's amendment received on 08/24/2005.

Claims 2 and 4 have been amended.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Erisson (USP 6,628,923).

Regarding claim 1, Erisson teaches a filter characteristic measuring method (e.g. Col.8, lines 20-44), comprising the steps of: generating an impulse signal (e.g. Col.16, lines 12-15); applying the impulse signal (reference signal or impulse signal) to a DUT (12) having an analog filter through a digital channel (waveform generator 14) (e.g. Col.2, lines 39-56, Col.3, lines 33-34); and measuring a gain of the analog filter in the DUT and a frequency characteristic by using an output of the analog filter (e.g. Col.3, lines 35-44).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Erisson (USP 6,628,923) in view of Dieterich (USP 5,208,596).

Regarding claim 2-3, Erisson fails to teach the analog filter is an equalizing filter and applying impulse signal to an equalizing filter and performing a differential and a fast Fourier transform (FFT) operation on output response of the equalizing filter, and measuring a boosting gain and a frequency response.

Dieterich teaches the analog filter is an equalizing filter (15, Fig.2) and applying impulse signal to an equalizing filter (e.g. Col.4, lines 5-12) and performing a differential and a fast Fourier transform (FFT) operation on output response of the equalizing filter, and measuring a boosting gain and a frequency response (e.g. Col.4, lines 5-38, Col.4, lines 51-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include an equalizing filter and applying impulse signal to an equalizing filter and performing a differential and a fast Fourier transform (FFT) operation on output response of the equalizing filter, and measuring a boosting gain and a frequency response as taught by Dieterich in a system for measuring a characteristic of a filter in a DUT of Erisson for the purpose of providing a frequency response, wherein the frequency response is the impulse response.

6. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Erisson (USP 6,628,923) in view of Becker et al. (USP 5,929,628).

Regarding claim 4, Erisson teaches system for measuring a characteristic of a filter in a DUT employing an analog filter (e.g. Col.3, lines 27-44), said system comprising: a digital channel (waveform generator 14) for providing an impulse signal without applying a sine wave (reference signal or impulse signal) to the analog filter (digital-to-analog filter) of DUT (e.g. Col.2, lines 39-56; Col.3, lines 33-34); a digitizer (processor 18, memory 22, digital filter 20) for receiving an output signal of the analog filter (digital-to-analog filter) so as to measure the characteristic of the filter ((e.g. Col.3, lines 35-44)).

Erisson fails to teach a controller for controlling the digital channel and the digitizer.

Becker et al. teach a controller (206) for controlling the digital channel (212) and the digitizer (220)(see Fig.2A).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a controller for controlling the digital channel and the digitizer as taught by Becker et al. in a system for measuring a characteristic of a filter in a DUT of Erisson for the purpose of providing a tester that can automatically correct signal amplitude error introduced in its channel and data acquisition circuitry (Becker et al., Col.3, lines 14-17).

Regarding claim 5, Erisson fails to teach the digitizer comprises: an anti-aliasing filter for antialiasing-filtering an output of the filter; an analog to digital (A/D) converter

for converting a filter output outputted from the anti-aliasing filter into digital data; a memory for capturing the digital data outputted from the A/D converter at a determined storage region; a digital signal processing (DSP) for processing in signal the digital data captured at the memory; and a digital filter for receiving the process signal outputted from the DSP and digitally filtering the process signal..

Becker et al. teach the digitizer comprises: an anti-aliasing (287); an analog to digital (A/D) converter (260); a memory (262); a digital signal processing (DSP); and a digital filter (208)(e.g. Fig.2A, Col.8, lines 20-29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include an anti-aliasing (287); an analog to digital (A/D) converter (260); a memory (262); a digital signal processing (DSP); and a digital filter (208) as taught by Becker et al. in a system for measuring a characteristic of a filter in a DUT of Erisson for the purpose of providing a tester that can automatically correct signal amplitude error introduced in its channel and data acquisition circuitry (Becker et al., Col.3, lines 14-17).

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Erisson (USP 6,628,923) in view of Becker et al. (USP 5,929,628) as applied to claim 4 above, and further in view of Dieterich (USP 5,208,596).

Regarding claim 6, Erisson in view of Becker et al. fail to teach the analog filter is an equalizing filter.

Dieterich teaches the analog filter is an equalizing filter (15, Fig.2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include an equalizing filter as taught by Dieterich in a system for measuring a characteristic of a filter in a DUT of Erisson in view of Becker et al. for the purpose of providing a frequency response, wherein the frequency response is the impulse response.

Response to Arguments

8. Applicant's arguments filed 08/24/2005 have been fully considered but they are not persuasive.

-Applicant argues that the prior did not teach "applying the impulse signal to a DUT having an analog filter through a digital channel; and measuring a gain of the analog filter in the DUT and a frequency characteristic by using an output of the analog filter" as cited in claim 1.

Examiner position is that Erisson teaches applying the impulse signal (reference signal or impulse signal) to a DUT (12) having an analog filter through a digital channel (waveform generator 14) (e.g. Col.2, lines 39-56, Col.3, lines 33-34); and measuring a gain of the analog filter in the DUT and a frequency characteristic by using an output of the analog filter (e.g. Col.3, lines 35-44).

-Applicant argues that the prior did not teach, "system for measuring a characteristic of a filter in a DUT employing an analog filter, said system comprising: a digital channel for providing an impulse signal without applying a sine wave to the analog filter of DUT" as cited in claim 4.

comprising: a digital channel (waveform generator 14) for providing an impulse signal without applying a sine wave (reference signal or impulse signal) to the analog filter (digital-to-analog filter) of DUT (e.g. Col.2, lines 39-56, Col.3, lines 33-34).

-Applicant argues that the prior did not teach, "performing a differential and a fast Fourier transform (FFT) operation on output response of the equalizing filter" as cited in claim 3.

Examiner position is that Dieterich teaches performing a differential and a fast Fourier transform (FFT) operation on output response of the equalizing filter, and measuring a boosting gain and a frequency response (e.g. Col.4, lines 5-38, Col.4, lines 51-61).

Conclusion

9. Specifically Erisson, Becker et al., and Dieterich have been added to second ground of rejection.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John H. Le whose telephone number is 571 272 2275. The examiner can normally be reached on 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Barlow can be reached on 571 272 2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JL
John H. Le

Patent Examiner-Group 2863
October 10, 2005

Michael Nghiem
MICHAEL NGHIEM
PRIMARY EXAMINER